afero

Firmware Specification

Preferred Pin Mappings

For Nordic nRF52 BLE Chipsets

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1. Introduction

Off-the-shelf modules, such as those for the nRF52832 BLE chipset, expose varying numbers of pins for the end-user. To support these different configurations with a single core firmware image, Afero factors out the pin mapping implementation details into a separate structure stored in flash. This way different pin map configurations can be bundled with the factory programming package, similar to the way device profiles are handled. The Afero generic firmware will read this pin map table at boot (runtime) to determine which pins are used.

This document specifies the suggested pin mappings for various module manufacturers that Afero has bundled by default with the firmware. Note that these mappings can only be programmed into a module using the Afero Factory Programmer; they cannot be updated over-the-air.

If your device requires a different mapping, please let the Afero Customer Enablement (ACE) team know well in advance. Afero will work with you to create a pin map binary that can be bundled along with the core firmware into your Afero Factory Programmer package.

2. Manufacturers

2.1 Taiyo Yuden

2.1.1 EYSHCNZWZ

FUNCTION	PIN LOCATION	PORT	NOTES
GPIO0/ANALOG0	34	P0.02 / AIN0	
GPIO1/ANALOG1	35	P0.03 / AIN1	
GPIO2/ANALOG2	6	P0.04 / AIN2	
GPIO3/ANALOG3	7	P0.05 / AIN3	
GPIO4/ANALOG4	30	P0.28 / AIN4	Unsupported in FW - future expansion.
GPIO5/ANALOG5	31	P0.29 / AIN5	Unsupported in FW - future expansion.
GPIO6/ANALOG6	32	P0.30 / AIN6	Unsupported in FW - future expansion.
GPIO7/ANALOG7	33	P0.31 / AIN7	Unsupported in FW - future expansion.
SCL	19	P0.18	For Afero HSM. Add 4.7k pullup to VIO.
SDA	39	P0.16	For Afero HSM. Add 4.7k pullup to VIO.
SPI_SCLK	24	P0.22	
SPI_MOSI	25	P0.23	
SPI_MISO	26	P0.24	
SPI_CS	27	P0.25	
HOST_INT_B	28	P0.26	
DEBUG_UART_TX	37	P0.12	
DEBUG_UART_RX	17	P0.14	
DEBUG_UART_RTS	38	P0.15	
DEBUG_UART_CTS	18	P0.17	
RESET_N	20	P0.21	Add 100k pullup to VIO.
SWDCLK	15		
SWDIO	14		

NOTE:

- P0.25 and P0.26 (Pins 27 and 28) need 12pF C0G/NP0 caps to ground per Nordic Errata #138.

2.2 Murata

2.2.1 MBN52832

FUNCTION	PIN LOCATION	PORT	NOTES
GPIO0/ANALOG0	12	P0.04 / AIN2	
GPIO1/ANALOG1	11	P0.03 / AIN1	
GPIO2/ANALOG2	10	P0.05 / AIN3	
GPIO3/ANALOG3	9	P0.02 / AIN0	
GPIO4/ANALOG4	27	P0.20	Unsupported in FW - future expansion.
GPIO5/ANALOG5	28	P0.17	Unsupported in FW - future expansion.
GPIO6/ANALOG6			Unsupported in FW - future expansion.
GPIO7/ANALOG7			Unsupported in FW - future expansion.
SCL	22	P0.18	For Afero HSM. Add 4.7k pullup to VIO.
SDA	23	P0.16	For Afero HSM. Add 4.7k pullup to VIO.
SPI_SCLK	1	P0.09	
SPI_MOSI	14	P0.07	
SPI_MISO	15	P0.08	
SPI_CS	13	P0.29	
HOST_INT_B	29	P0.13	
DEBUG_UART_TX	2	P0.06	
DEBUG_UART_RX	25	P0.14	
DEBUG_UART_RTS	26	P0.10	
DEBUG_UART_CTS	24	P0.15	
RESET_N	17	P0.21	Add 100k pullup to VIO.
SWDCLK	18		
SWDIO	16		

NOTES:

- A 32kHz crystal is needed on P0.00/3 and P0.01/4 as per the Murata datasheet and dev board.
- An external matching network is required per the Murata datasheet. This MUST match Murata's recommendations to maintain compliance with their certifications.
- GPIOs 4 and 5 are not analog capable.

2.3 Rigado

2.3.1 BMD300/301

FUNCTION	PIN LOCATION	PORT	NOTES
GPIO0/ANALOG0	15	P0.02 / AIN0	
GPIO1/ANALOG1	19	P0.03 / AIN1	
GPIO2/ANALOG2	20	P0.04 / AIN2	
GPIO3/ANALOG3	21	P0.05 / AIN3	
GPIO4/ANALOG4	9	P0.28 / AIN4	Unsupported in FW - future expansion.
GPIO5/ANALOG5	10	P0.29 / AIN5	Unsupported in FW - future expansion.
GPIO6/ANALOG6	11	P0.30 / AIN6	Unsupported in FW - future expansion.
GPIO7/ANALOG7	12	P0.31 / AIN7	Unsupported in FW - future expansion.
SCL	36	P0.18	For Afero HSM. Add 4.7k pullup to VIO.
SDA	34	P0.16	For Afero HSM. Add 4.7k pullup to VIO.
SPI_SCLK	40	P0.22	
SPI_MOSI	41	P0.23	
SPI_MISO	42	P0.24	
SPI_CS	37	P0.19	
HOST_INT_B	38	P0.20	
DEBUG_UART_TX	28	P0.12	
DEBUG_UART_RX	32	P0.14	
DEBUG_UART_RTS	33	P0.15	
DEBUG_UART_CTS	35	P0.17	
RESET_N	39	P0.21	Add 100k pullup to VIO.
SWDCLK	43		
SWDIO	44		

NOTE:

- A 32kHz crystal is needed on P0.00/13 and P0.01/14 as per the Rigado datasheet and dev board.

2.3.2 BMD350

FUNCTION	PIN LOCATION	PORT	NOTES
GPIO0/ANALOG0	28	P0.02 / AIN0	
GPIO1/ANALOG1	44	P0.03 / AIN1	
GPIO2/ANALOG2	27	P0.04 / AIN2	
GPIO3/ANALOG3	21	P0.05 / AIN3	
GPIO4/ANALOG4	45	P0.28 / AIN4	Unsupported in FW - future expansion.
GPIO5/ANALOG5	31	P0.29 / AIN5	Unsupported in FW - future expansion.
GPIO6/ANALOG6	29	P0.30 / AIN6	Unsupported in FW - future expansion.
GPIO7/ANALOG7	30	P0.31 / AIN7	Unsupported in FW - future expansion.
SCL	8	P0.18	For Afero HSM. Add 4.7k pullup to VIO.
SDA	9	P0.16	For Afero HSM. Add 4.7k pullup to VIO.
SPI_SCLK	32	P0.27	
SPI_MOSI	35	P0.23	
SPI_MISO	36	P0.24	
SPI_CS	33	P0.25	
HOST_INT_B	34	P0.26	
DEBUG_UART_TX	13	P0.12	
DEBUG_UART_RX	14	P0.14	
DEBUG_UART_RTS	11	P0.15	
DEBUG_UART_CTS	10	P0.17	
RESET_N	7	P0.21	Add 100k pullup to VIO.
SWDCLK	4		
SWDIO	5		

NOTES:

- A 32kHz crystal is needed on P0.01/23 and P0.00/24 as per the Rigado datasheet and dev board.
- P0.25 and P0.26 (Pins 33 and 34) need 12pF C0G/NP0 caps to ground per Nordic Errata #138.

3. Sample HSM Schematic